What Is Claimed Is:

1. A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch associated with said non-volatile memory; and

enabling an error correction coding circuit during reading of said repairing data to thereby identify and repair defective columns or rows associated with said non-volatile memory regardless of the corruption of said columns or rows.

2. The method of claim 1 further comprising the step of:

enabling said error correction coding circuit during an access of a main array associated with said non-volatile memory to thereby correct correctable errors if a particular address corresponds to an address of at least one defective column or row.

3. The method of claim 2 wherein said particular address comprises a Y-address corresponding to said at least one defective column or row.

4. The method of claim 1 further comprising the step of:

linking a read circuit to said main array to thereby permit data to be read from said main array and transmitted to said error correction coding circuit;

connecting said error control circuit to said volatile latch to thereby permit data to be transferred from said error correction coding circuit to said volatile latch; and

linking a decoder circuit to said error correction coding circuit, such that said decoder circuit is linked to said information array, at least one spare row, and said main array, wherein said main array includes a normal array and at least one spare column.

5. The method of claim 4 further comprising the step of:

linking said volatile latch to said decoder circuit to thereby permit data contained within said volatile latch to be accessed by said decoder circuit.

6. The method of claim 1 further where in the step of reading repairing data from an information array associated with said non-volatile memory to a volatile latch associated with said non-volatile memory, further comprises the steps of:

accessing said repairing data contained within said information array following initialization of a computer system associated with said non-volatile memory; and

thereafter transferring said column-repairing data to said non-volatile memory.

7. A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch associated with said non-volatile memory; and

enabling an error correction coding circuit during an access of a main array associated with said non-volatile memory to thereby correct correctable errors if a particular address corresponds to an address of at least one defective column or row, wherein said particular address comprises a Y-address corresponding to said at least one defective column or row.

8. A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch associated with said non-volatile memory, wherein said column repair data is read utilizing a read circuit linked to a main array associated with said non-volatile memory and an error correction coding circuit linked to said volatile latch and a decoder circuit; and

enabling said error correction coding circuit during an access of said main array to thereby correct correctable errors if a particular address corresponds to an address of at least one defective column or row, wherein said particular address comprises a Y-address corresponding to said at least one defective column or row.

9. A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch associated with said non-volatile memory, wherein said column repair data is read utilizing a read circuit linked to a main array associated with said non-volatile memory and an error correction coding circuit linked to said volatile latch and a decoder circuit; and

enabling said error correction coding circuit during reading of said repairing data to thereby identify and repair defective columns or rows associated with said non-volatile memory regardless of the corruption of said columns or rows.

10. A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch associated with said non-volatile memory following initialization of a computer system associated with said non-volatile memory, wherein said column repair data is read utilizing a read circuit linked to a main array associated with said non-volatile memory and an error correction coding circuit linked to said volatile latch and a decoder circuit; and

enabling said error correction coding circuit during reading of said repairing data to thereby identify and repair defective columns or rows associated with said non-volatile memory regardless of the corruption of said columns or rows.

11. A system for improving repairing efficiency in a non-volatile memory, said system comprising:

reading circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch associated with said non-volatile memory; and

an error correction coding circuit enabled during reading of said repairing data to thereby identify and repair defective columns or rows associated with said non-volatile memory regardless of the corruption of said columns or rows.

12. The system of claim 11 further comprising :

said error correction coding circuit enabled during an access of a main array associated with said non-volatile memory to thereby correct correctable errors if a particular address corresponds to an address of at least one defective column or row.

13. The system of claim 12 wherein said particular address comprises a Y-address corresponding to said at least one defective column or row.

14. The system of claim 11 further comprising:

said read circuit linked to said main array to thereby permit data to be read from said main array and transmitted to said error correction coding circuit;

said error control circuit connected to said volatile latch to thereby permit data to be transferred from said error correction coding circuit to said volatile latch; and

a decoder circuit linked to said error correction coding circuit, such that said decoder circuit is linked to said information array, at least one spare row, and said main array, wherein said main array includes a normal array and at least one spare column.

15. The system of claim 14 further comprising :

said volatile latch linked to said decoder circuit to thereby permit data contained within said volatile latch to be accessed by said decoder circuit.

16. The system of claim 11 wherein:

said repairing data contained within said information array is accessed following initialization of a computer system associated with said non-volatile memory, thereby resulting in the transfer of said repairing data to said non-volatile memory.

17. A system for improving repairing efficiency in a non-volatile memory, said system comprising:

read circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch associated with said non-volatile memory; and

an error correction coding circuit enabled during an access of a main array associated with said non-volatile memory to thereby correct correctable errors if a particular address corresponds to an address of at least one defective column, wherein said particular address comprises a Y-address corresponding to said at least one defective column or row.

18. A system for improving repairing efficiency in a non-volatile memory, said system comprising:

read circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch associated with said non-volatile memory, wherein said column repair data is read utilizing a read circuit linked to a main array associated with said non-volatile memory and an error correction coding circuit linked to said volatile latch and a decoder circuit; and

said error correction coding circuit enabled during an access of said main array to thereby correct correctable errors if a particular address corresponds to an address of at least one defective column, wherein said particular address comprises a Y-address corresponding to said at least one defective column or row.

19. A system for improving repairing efficiency in a non-volatile memory, said system comprising:

a read circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch associated with said non-volatile memory, wherein said column repair data is read utilizing a read circuit linked to a main array associated with said non-volatile memory and an error correction coding circuit linked to said volatile latch and a decoder circuit; and

said error correction coding circuit enabled during reading of said repairing data to thereby identify and repair defective columns or rows associated with said non-volatile memory regardless of the corruption of said columns or rows.

20. A system for improving repairing efficiency in a non-volatile memory, said system comprising:

a read circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch associated with said non-volatile memory following initialization of a computer system associated with said non-volatile memory, wherein said column repair data is read utilizing a read circuit linked to a main array associated with said non-volatile memory and an error correction coding circuit linked to said volatile latch and a decoder circuit; and

said error correction coding circuit enabled during reading of said repairing data to thereby identify and repair defective columns or rows associated with said non-volatile memory regardless of the corruption of said columns or rows.